



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

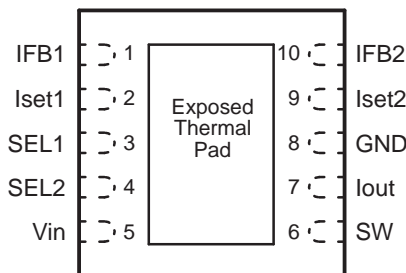
ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾	OVP (Typ.)	PACKAGE MARKING
-40 to 85°C	TPS61150DRCR	28 V	BCQ
-40 to 85°C	TPS61151DRCR	22 V	BRH
-40 to 85°C	TPS61150DRCT	28 V	BCQ
-40 to 85°C	TPS61151DRCT	22 V	BRH

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

DEVICE INFORMATION

10 pin 3*3 mm QFN PACKAGE
(TOP VIEW)



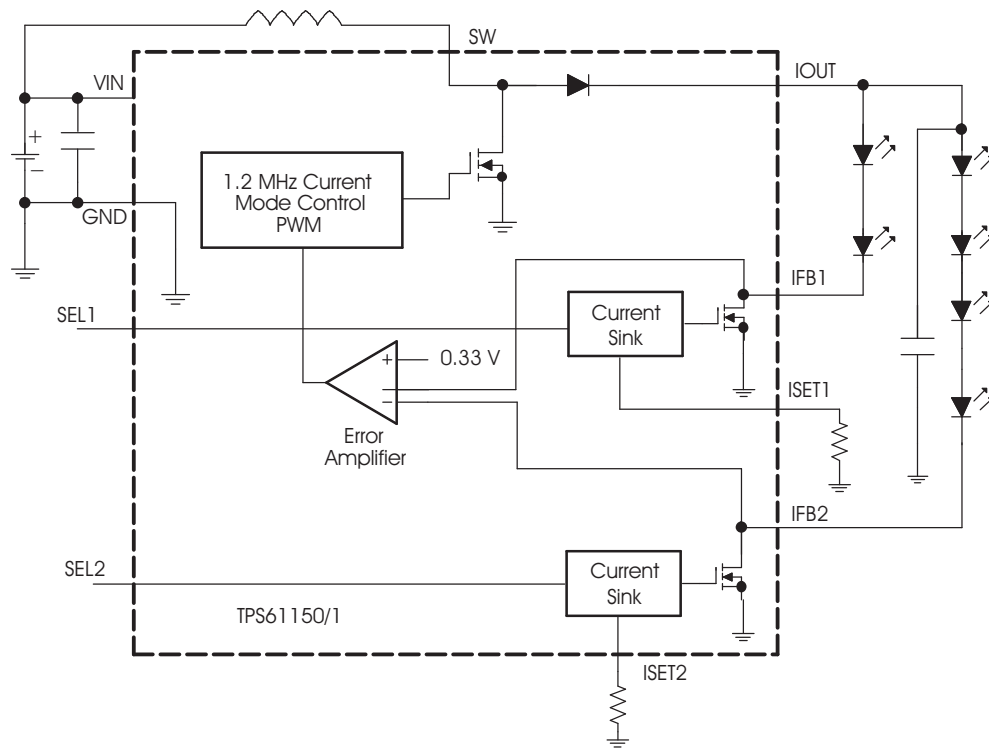
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Vin	5	I	The input pin to the IC. It provides the current to the boost power stage, and also powers the IC circuit. When Vin is below the undervoltage lockout threshold, the IC turns off and disables outputs; thereby disconnecting the WLEDs from the input.
GND	8	O	The ground of the IC. Connect the input and output capacitors very close to this pin.
SW	6	I	This is the switching node of the IC.
Iout	7	O	The output of the constant current supply. It is directly connected to the boost converter output.
IFB1, IFB2	10	I	The return path for the Iout regulation. Current regulator is connected to this pin, and it can be disabled to open the current path.
ISET1, ISET2	2 9	I	Output current programming pin. The resistor connected to the pin programs its corresponding output current.
SEL1, SEL2	3 4	I	Mode selection pins. See Table 1 for details.
Thermal Pad			The thermal pad should be soldered to the analog ground. If possible, use thermal via to connect to ground plane for ideal power dissipation.

Table 1. TPS61150/1 Mode Selection

SEL1	SEL2	IFB1	IFB2
H	L	Enable	Disable
L	H	Disable	Enable
H	H	Enable	Enable
L	L	IC Shutdown	

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Supply voltages on pin VIN ⁽²⁾	-0.3 to 7	V
Voltages on pins SEL1/2, ISET1/2 ⁽²⁾	-0.3 to 7	V
Voltage on pin IOUT, SW, IFB1 and IFB2 ⁽²⁾	30	V
Continuous power dissipation	See Dissipation Rating Table	
Operating junction temperature range	-40 to 150	°C
Storage temperature range	-65 to 150	°C
Lead Temperature (soldering, 10 sec)	260	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	R _{θJA}	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
QFN ⁽¹⁾	270°C/W	370 mW	204 mW	148 mW
QFN ⁽²⁾ (2)	48.7°C/W	2.05 W	1.13 W	821 mW

- (1) Soldered PowerPAD on a standard 2-layer PCB without vias for thermal pad.
- (2) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad .

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _I	Input voltage range	2.5		6	V
V _O	Output voltage range	V _{in}		27	V
L	Inductor ⁽¹⁾		10		μH
C _i	Input capacitor ⁽¹⁾	1			μF
C _O	Output capacitor ⁽¹⁾	1			μF
T _A	Operating ambient temperature	–40		85	°C
T _J	Operating junction temperature	–40		125	°C

(1) See Application Section for further information.

ELECTRICAL CHARACTERISTICS

$V_I = 3.6\text{ V}$, $SELx = Vin$, $R_{set} = 80\text{ k}\Omega$, $V_{IO} = 15\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range		2.5		6	V
I_Q	Operating quiescent current into V_{in}	Device PWM switching no load			2	mA
I_{SD}	Shutdown current	$SELx = GND$			1.5	μA
V_{UVLO}	Undervoltage lockout threshold	V_{in} falling		1.65	1.8	V
V_{hys}	Undervoltage lockout hysteresis			70		mV
ENABLE AND SOFT START						
$V_{(selh)}$	SEL logic high voltage	$V_{in} = 2.7\text{ V}$ to 6 V	1.2			V
$V_{(sello)}$	SEL logic low voltage	$V_{in} = 2.7\text{ V}$ to 6 V			0.4	V
$R_{(en)}$	SEL pull down resistor		300	700		$\text{k}\Omega$
T_{off}	SEL pulse width to disable	$SELx$ high to low	40			ms
K_{ss}	IFB soft start current steps			16		
T_{ss}	Soft start time step	Measured as clock divider		64		
T_{ss_en}	Soft start enable time	Time between falling and rising of two adjacent $SELx$ pulses	40			ms
CURRENT FEEDBACK						
$V_{(ISET)}$	ISET pin voltage		1.204	1.229	1.254	V
$K_{(ISET)}$	Current multiplier	I_{out}/I_{set}	820	900	990	
K_M	Current matching	In reference to the average of two output current	-6		6	%
$V_{(IFB)}$	IFB Regulation voltage		300	330	360	mV
$V_{(IFB_L)}$	IFB low threshold hysteresis			60		mV
T_{isink}	Current sink settle time measured from $SELx$ rising edge ⁽¹⁾				6	μs
I_{lkg}	IFB pin leakage current	IFB voltage = 25 V			1	μA
POWER SWITCH AND DIODE						
$r_{DS(on)}$	N-channel MOSFET on-resistance	$V_{IN} = V_{GS} = 3.6\text{ V}$		0.6	0.9	Ω
$I_{(LN_NFET)}$	N-channel leakage current	$V_{DS} = 25\text{ V}$			1	μA
V_F	Power diode forward voltage	$I_d = 0.7\text{ A}$		0.83	1.0	V
OC AND OVP						
I_{LIM}	N-Channel MOSFET current limit	Dual output, $I_{out}=15\text{ V}$, $D=76\%$	0.75	1.0	1.25	A
		Single output, $I_{out}=15\text{ V}$, $D=76\%$	0.40	0.55	0.7	
$I_{(IFB_MAX)}$	Current sink max output current	IFB = 330 mV	35			mA
V_{OVP}	Overvoltage threshold	TPS61150	27	28	29	V
		TPS61151	21	22	23	
$V_{OVP(hys)}$	Overvoltage hysteresis	TPS61150		550		mV
		TPS61151		440		
PWM AND PFM CONTROL						
f_S	Oscillator frequency		1.0	1.2	1.5	MHz
D_{max}	Maximum duty cycle	$V_{FB} = 1\text{ V}$	90	93		%
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		$^\circ\text{C}$
T_{hys}	Thermal shutdown threshold hysteresis			15		$^\circ\text{C}$

(1) This specification determines the minimum on time required for PWM dimming for desirable linearity. The maximum PWM dimming frequency can be calculated from the minimum duty cycle required in the application.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURES
Overcurrent Limit	Vin = 3 V, 3.6 V, and 4 V, Single and dual output	1,2
WLED efficiency	Vin = 3.3 V, 3.6 V and 4 V, 3 WLED, WLED voltage= 11 V	3
WLED efficiency	Vin = 3.3 V, 3.6 V and 4 V, 4 WLED, WLED voltage = 15 V	4
WLED efficiency	Vin = 3.3 V, 3.6 V and 4 V, 5 WLED, WLED voltage = 19 V	5
WLED efficiency	Vin = 3.3 V, 3.6 V and 4 V, 6 WLED, WLED voltage= 23 V	6
Both on efficiency	Vin = 3.3 V, 3.6 V and 4 V, 4 WLED on each output	7
K value over current	Vin = 3.6 V, Iload = 2 mA to 25 mA	8
PWM dimming linearity	Frequency = 20 kHz and 30 KHz	9
Single output PWM dimming waveform		10
Multiplexed PWM dimming waveform		11
Start up waveform		12

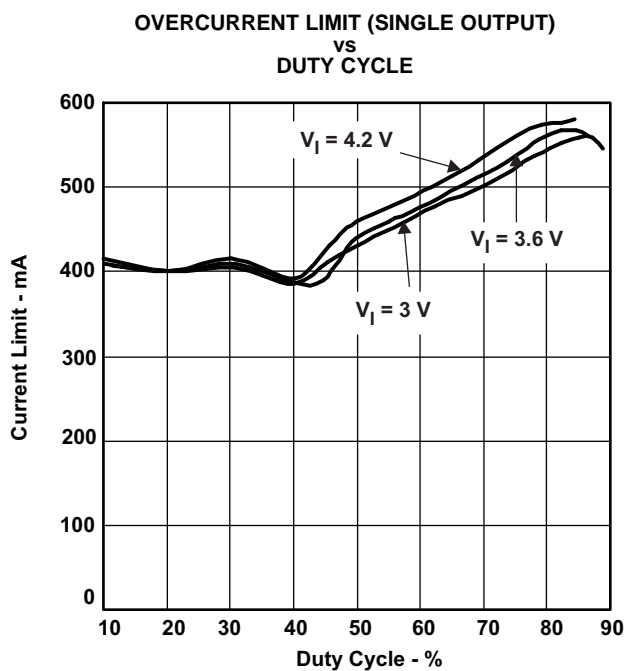


Figure 1.

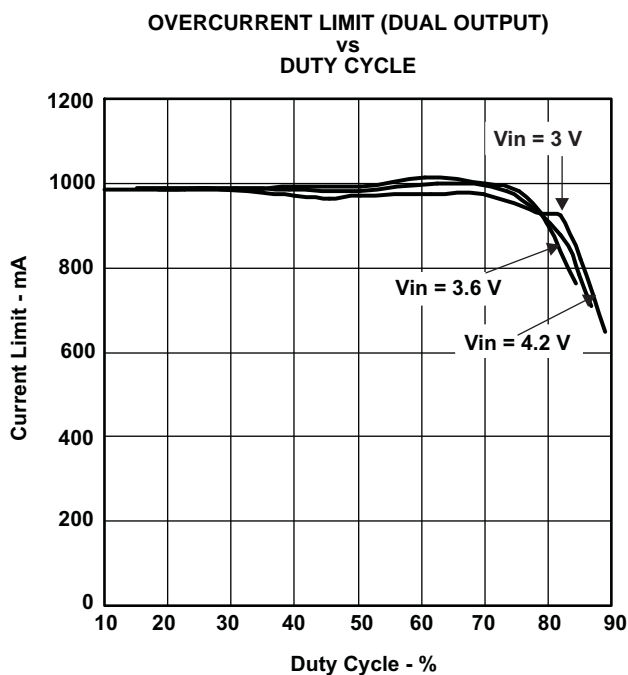


Figure 2.

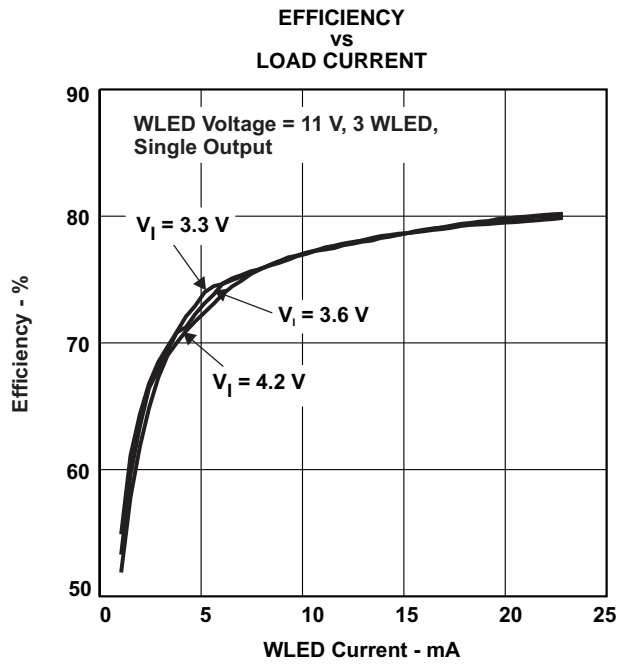


Figure 3.

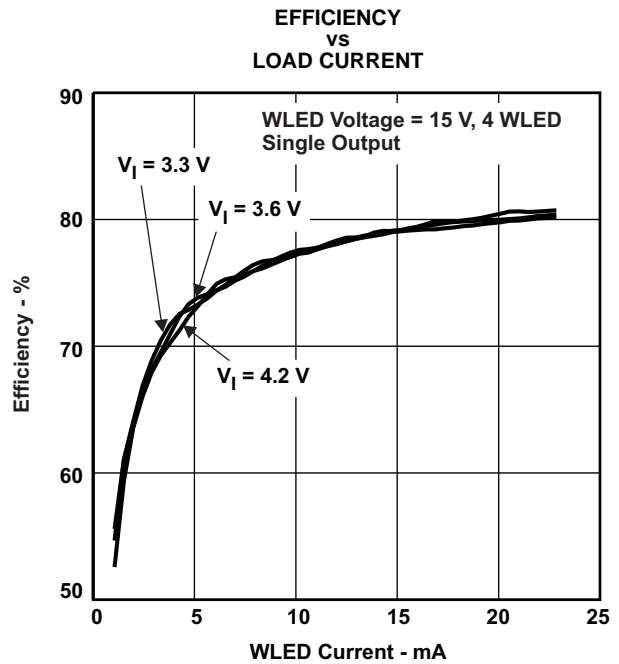


Figure 4.

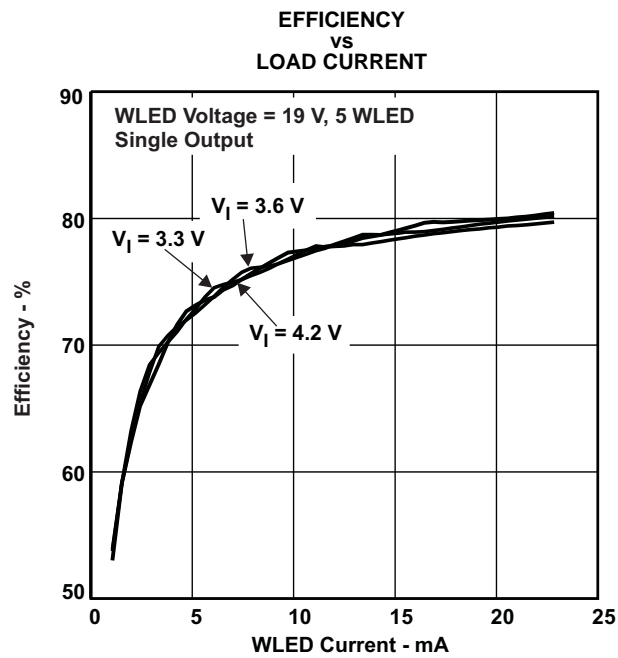


Figure 5.

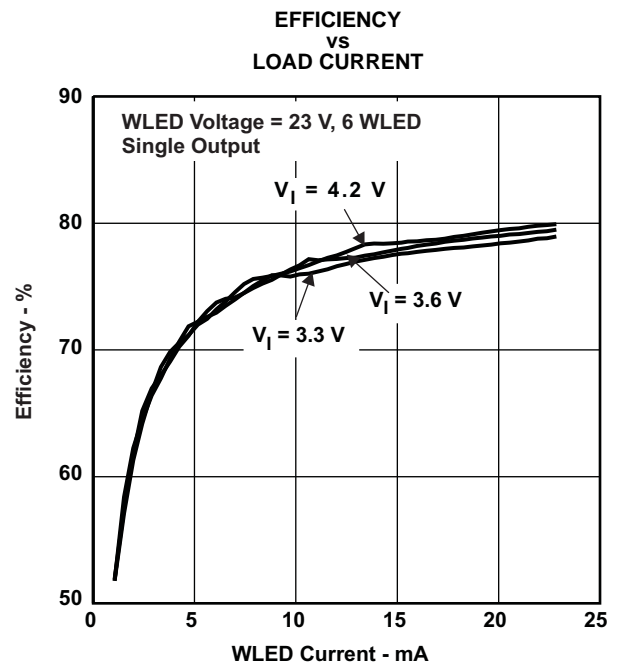


Figure 6.

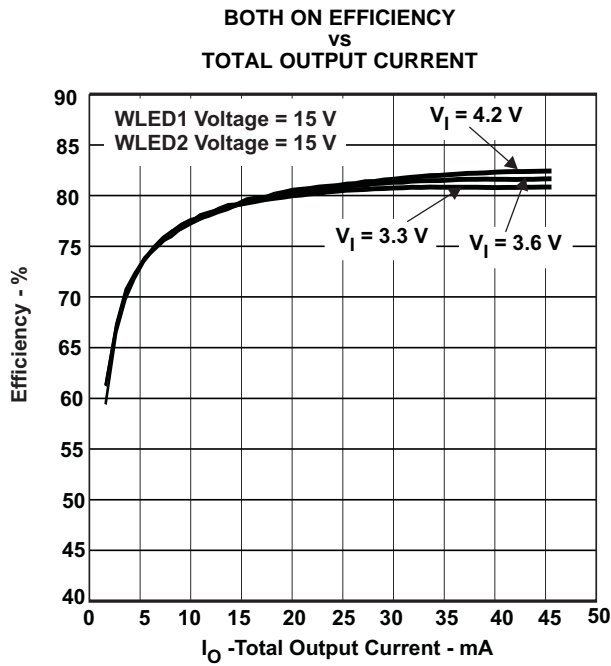


Figure 7.

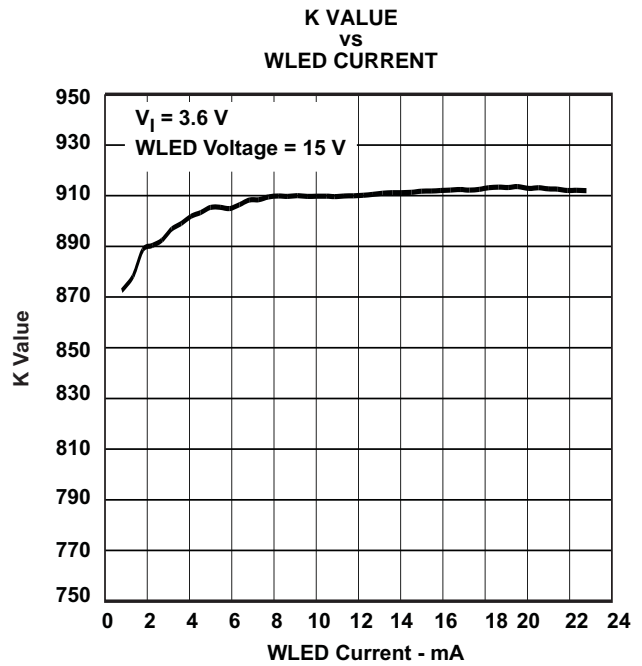


Figure 8.

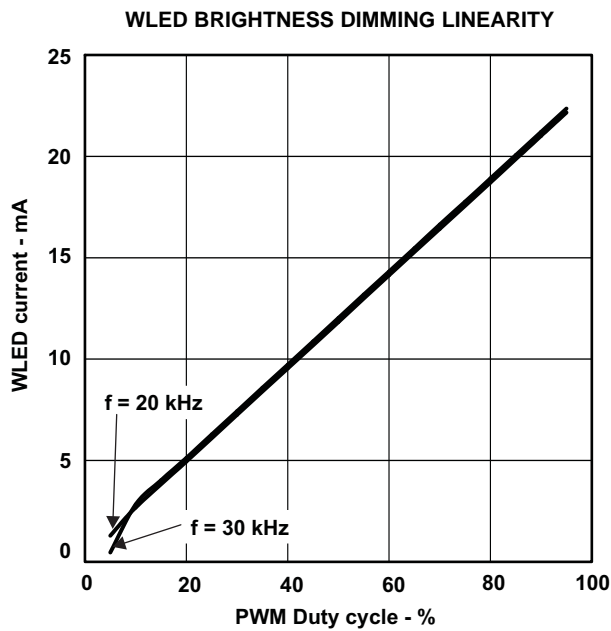


Figure 9.

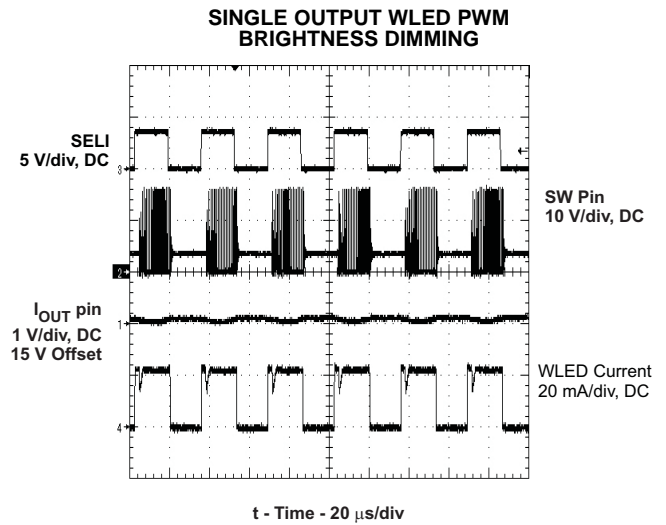


Figure 10.

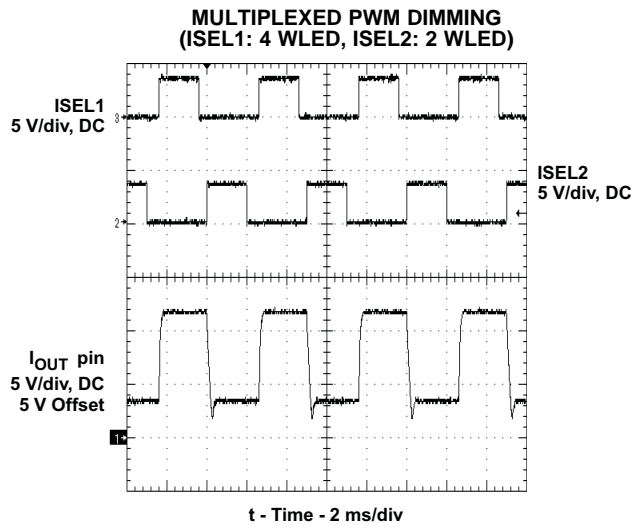


Figure 11.

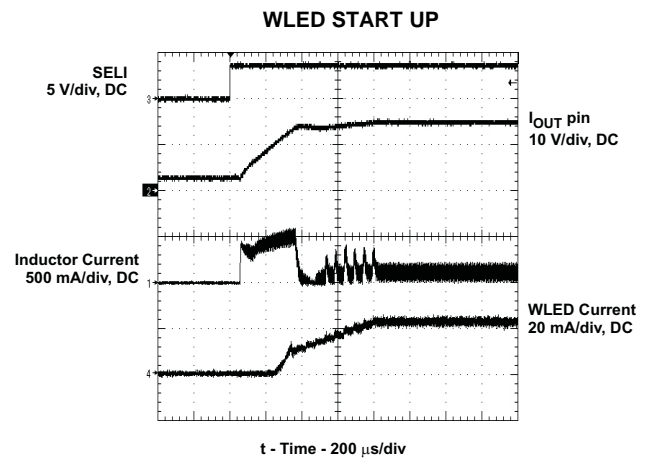


Figure 12.

DETAILED DESCRIPTION

CURRENT REGULATION

The TPS61150/1 uses a single boost regulator to drive 2 WLED strings whose current can be programmed independently. The boost converter adopts PWM control which is ideal for high output current and low output ripple noises. The feedback loop regulates the IFB pin to a threshold voltage (330 mV typical), giving the current sink circuit just enough headroom to operate.

The regulation current is set by the resistor on the Iset pin based on

$$I_O = \frac{V_{ISET}}{R_{SET}} \times K_{ISET} \quad (1)$$

where

I_o = output current

V_{ISET} = Iset pin voltage (1.229 V typical)

R_{SET} = Iset pin resistor value

K_{ISET} = current multiplier (900 typical)

When both outputs are enabled, the boost converter regulates to the IFB pin that demands higher Iout pin voltage, $V(I_{OUT})$, and let the other IFB pin rise above its regulation voltage. The feedback path dynamically switches to the other IFB pin if its voltage drops more than the IFB low hysteresis (60 mV typical) below its regulation voltage. This ensures proper current regulation for both outputs. When both IFB voltages are low, IFB1 is used for regulation. Once IFB1 reaches its regulation voltage, the feedback path may hand over to IFB2 if it is still low, and the boost output will continue to rise.

The overall efficiency in this mode depends on the voltage different between the IFB1 and IFB2. A large difference reduces the efficiency due to power losses across the current sink circuit. To improve the efficiency of the both-on mode, the two current outputs can be turned on complementarily by applying out of phase enable signal to the SEL pins. The ISET pin resistors need to be recalculated to compensate for the reduced dc current.

START UP

During start up, both the boost converter and the current sink circuitry are trying to establish steady state simultaneously. The current sink circuitry ramps up current in 16 steps, with each step taking 64 clock cycles. This ensures that the current sink loop is slower than the boost converter response during startup. Therefore, the boost converter output comes up slowly as current sink circuitry ramps up the current. This ensures smooth start up and minimizes in-rush current.

OVERVOLTAGE PROTECTION

To prevent the boost output run away as the result of WLED disconnection, there is an overvoltage protection circuit which stops the boost converter from switching as soon as its output exceeds the OVP threshold. When the voltage falls below the OVP threshold, the converter resumes switching.

The two OVP options offer the choices to prevent a 25 V rated output capacitor or the internal 30 V FET from breaking down.

UNDERVOLTAGE LOCKOUT

An internal thermal shutdown circuit turns off the IC when the typical junction temperature of 160°C is exceeded. The thermal shutdown has a hysteresis of typically 15°C.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the IC when the typical junction temperature of 160°C is exceeded. The thermal shutdown has a hysteresis of typically 15°C.

DETAILED DESCRIPTION (continued)

ENABLE

Pulling either the SEL1 or SEL2 pin low turns off the corresponding output. If both SEL1 and SEL2 are low for more than 40 ms, the IC shuts down and consumes less than 1 μA current. The SEL pin can also be used for PWM brightness dimming. To improve PWM dimming linearity, soft start is disabled if the time between falling and rising edges of two adjacent SELx pulses is less than 40 ms. See APPLICATION INFORMATION for details.

Each SEL input pin has an internal pull down resistor to disable the device when the pin is floating.

APPLICATION INFORMATION

MAXIMUM OUTPUT CURRENT

The over-current limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit, input voltage, output voltage and efficiency can all change maximum current output. Since current limit clamps peak inductor current, ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$I_p = \frac{1}{\left[L \times \left(\frac{1}{V_{iout} + V_f - V_{in}} + \frac{1}{V_{in}} \right) \times F_s \right]} \tag{2}$$

where

I_p = inductor peak to peak ripple

L = inductor value

V_f = power diode forward voltage

F_s = switching frequency

V_{iout} = boost output voltage. It is equal to 330 mV + voltage drop across WLED.

$$I_{out_max} = \frac{V_{in} \times \left(I_{lim} - \frac{I_p}{2} \right) \times \eta}{V_{iout}} \tag{3}$$

where

I_{out_max} = maximum output current of the boost converter

I_{lim} = overcurrent limit

η = efficiency

To keep a tight range of the overcurrent limit, The TPS61150/1 uses the V_{in} and I_{out} pin voltage to compensate for the overcurrent limit variation caused by the slope compensation. However, the current threshold still has residual dependency on the V_{in} and I_{out} voltage. Use [Figure 1](#) and [Figure 2](#) to identify the typical overcurrent limit in your application, and use $\pm 25\%$ tolerance to account for temperature dependency and process variations.

The maximum output current can also be limited by the current capability of the current sink circuitry. It is designed to provide maximum 35 mA current regardless of the current capability of the boost converter.

WLED BRIGHTNESS DIMMING

There are three ways to change the output current *on the fly* for WLED dimming. The first method parallels an additional resistor with the ISET pin resistor as shown in [Figure 13](#) . The switch (Q1) can change the ISET pin resistance, and therefore modify the output current. This method is very simple, but can only provide limited dimming steps.

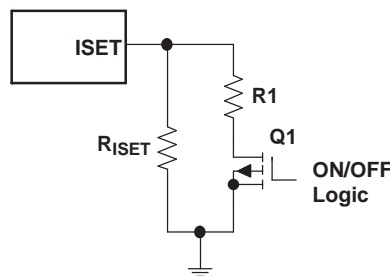


Figure 13. Switching In/Out an Additional Resistor to Change Output Current

APPLICATION INFORMATION (continued)

Alternatively, a PWM dimming signal at the SEL pin can modulate the output current by the duty cycle of the signal. The logic high of the signal turns on the current sink circuit, while the logic low turns it off. This operation creates an averaged DC output current proportional to the duty cycle of the PWM signal. The frequency of the PWM signal has to be high enough to avoid flashing of the WLEDs. The soft start of the current sink circuit is disabled during the PWM dimming to improve linearity.

The major concern of the PWM dimming is the creation of audible noises which can come from the inductor and/or output capacitor of the boost converter. The audible noises on the output capacitor are created by the presence of voltage ripple in range of audible frequencies. The TPS61150/1 alleviates the problem by disconnecting the WLEDs from the output capacitor when the SEL pin is low. Therefore, the output capacitor is not discharged by the WLEDs, which reduces the voltage ripple during PWM dimming.

The audible noises can be eliminated by using PWM dimming frequency above or below the audible frequency range. The maximum PWM dimming frequency of the TPS61150/1 is determined by the current settling time (T_{isink}) which is the time required for the circuit sink circuit to reach steady state after the SEL pin transitions from low to high. The maximum dimming frequency can be calculated by

$$F_{PWM_MAX} = \frac{D_{min}}{T_{isink}} \quad (4)$$

D_{min} = min duty cycle of the PWM dimming required in the application.

For 20% D_{min} , PWM dimming frequency up to 33 kHz is possible, making the noise frequency above the audible range.

The third method uses an external DC voltage and resistor as shown in [Figure 14](#) to change the ISET pin current, and thus control the output current. The DC voltage can be the output of a filtered PWM signal. The equation to calculate the output current is

$$I_{WLED} = K_{ISET} \times \left(\frac{1.229}{R_{ISET}} + \frac{1.229 - V_{DC}}{R_1} \right) \text{ for DC voltage input} \quad (5)$$

$$I_{WLED} = K_{ISET} \times \left(\frac{1.229}{R_{ISET}} + \frac{1.229 - V_{DC}}{R_1 + 10K} \right) \text{ for PWM signal input} \quad (6)$$

K_{ISET} = current multiplier between the ISET pin current and the IFB pin current.

VDC= voltage of the dc voltage source or the dc voltage of the PWM signal.



Figure 14. Analog Dimming Uses an External Voltage Source to Control the Output Current

INDUCTOR SELECTION

Because the selection of the inductor affects the power supply steady state operation, transient behavior and loop stability, the inductor is the most important component in power regulator design. There are three specifications most important to the performance of the inductor, inductor value, dc resistance and saturation current. Considering inductor value alone is not enough.

The inductor's inductance value determines the inductor ripple current. It is generally recommended to set peak to peak ripple current given by [Equation 2](#) to 30–40% of dc current. It is a good compromise of power losses and inductor size. For this reason, 10-μH inductors are recommended for TPS61150/1. Inductor dc current can be calculated as

APPLICATION INFORMATION (continued)

$$I_{L_DC} = \frac{V_{iout} \times I_{out}}{V_{in} \times \eta} \tag{7}$$

Use the maximum load current and minimum Vin for calculation.

The internal loop compensation for PWM control is optimized for the external component shown in the typical application circuit with consideration of component tolerance. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20 to 35% from the 0-A value depending on how the inductor vendor defines saturation. Using an inductor with a smaller inductance value forces discontinuous PWM in which inductor current ramps down to zero before the end of each switching cycle. It reduces the boost converter’s maximum output current, and causes large input voltage ripple. An inductor with larger inductance will reduce the gain and phase margin of the feedback loop, possibly resulting in instability

Regulator efficiency is dependent on the resistance of its high current path and switching losses associated with the PWM switch and power diode. Although the TPS61150/1 has optimized the internal switches, the overall efficiency still relies on inductor’s DC resistance (DCR); Lower DCR improves efficiency. However, there is a trade off between DCR and inductor size, and shielded inductors typically have higher DCR than unshielded ones. DCR in range of 150 mΩ to 350 mΩ is suitable for applications requiring both on mode. DCR in the range of 250 mΩ to 450 mΩ is a good choice for single output application. Table 2 and Table 3 list recommended inductor models.

Table 2. Recommended Inductors for Single Output

	L (μH)	DCR Typ (mΩ)	Isat (A)	SIZE (L×W×H mm)
TDK				
VLF3012AT-100MR49	10	360	0.49	2.8×3.0×1.2
VLCF4018T-100MR74-2	10	163	0.74	4.0×4.0×1.8
Sumida				
CDRH2D11/HP	10	447	0.52	3.2×3.2×1.2
CDRH3D16/HP	10	230	0.84	4.0×4.0×1.8

Table 3. Recommended Inductors for Dual Output

	L (μH)	DCR Typ (mΩ)	Isat (A)	SIZE (L×W×H mm)
TDK				
VLCF4018T-100MR74-2	10	163	0.74	4×4.0×1.8
VLF4012AT-100MR79	10	300	0.85	3.5×3.7×1.2
Sumida				
CDRH3D16/HP	10	230	0.84	4×4.0×1.8
CDRH4D11/HP	10	340	0.85	4.8×4.8×1.2

INPUT AND OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected for the output ripple of the converter. This ripple voltage is the sum of the ripple caused by the capacitor’s capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{out} = \frac{(V_{iout} - V_{in}) I_{out}}{V_{iout} \times F_s \times V_{ripple}} \tag{8}$$

V_{ripple} = Peak to peak output ripple.

For $V_{in} = 3.6\text{ V}$, $V_{out} = 20\text{ V}$, and $F_s = 1.2\text{ MHz}$, 0.1% ripple (20 mV) would require 1 μF capacitor. For this value, ceramic capacitors are the best choice for its size, cost and availability.

The additional output ripple component caused by ESR is calculated using:

$$V_{\text{ripple_ESR}} = I_{\text{out}} \times R_{\text{ESR}}$$

Due to its low ESR, $V_{\text{ripple_ESR}}$ can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

During a load transient, the capacitor at the output of the boost converter has to supply or absorb additional current before the inductor current ramps up the steady state value. Larger capacitors always help to reduce the voltage over and under shoot during a load transient. A larger capacitor also helps loop stability.

Care must be taken when evaluating a ceramic capacitor's derating due to applied dc voltage, aging and frequency response. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the range of TPS61150/1's switching frequency. So the effective capacitance is significantly lower. Therefore, it may be necessary to use small capacitors in parallel instead of one large capacitor.

The popular vendors for high value ceramic capacitors are:

TDK (<http://www.component.tdk.com/components.php>)

Murata (<http://www.murata.com/cap/index.html>)

Table 4. Recommended Input and Output Capacitors

	Capacitance (μF)	Voltage (V)	Case
TDK			
C3216X5R1E475K	4.7	25	1206
C2012X5R1E105K	1	25	805
C1005X5R0J105K	1	6.3	402
Murata			
GRM319R61E475KA12D	4.7	25	1206
GRM216R61E105KA12D	1	25	805
GRM155R60J105KE19D	1	6.3	402

LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor needs not only to be close to the V_{in} pin, but also to the GND pin in order to reduce the input ripple seen by the IC. The V_{in} and SW pins are conveniently located on the edges of the IC; therefore, the inductor can be placed close to the IC. The output capacitor needs to be placed near the load to minimize ripple and maximize transient performance.

It is also beneficial to have the ground of the output capacitor close to the GND pin since there will be large ground return current flowing between them. When laying out signal ground, it is recommended to use short traces separated from power ground traces, and connect them together at a single point.

ADDITIONAL APPLICATION CIRCUIT

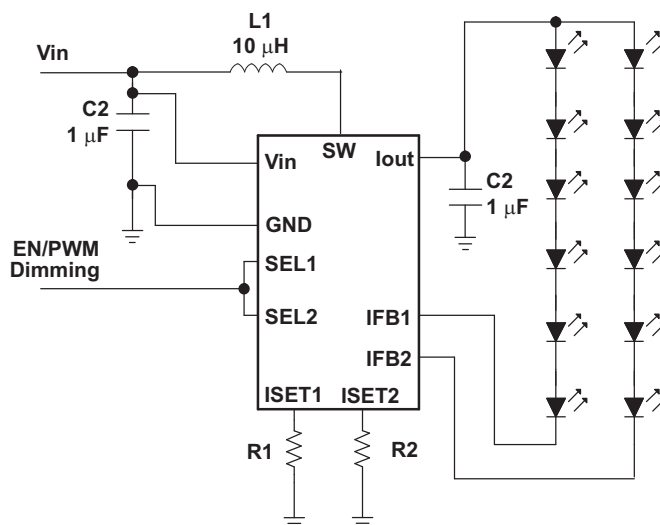


Figure 15. Driving Up to 12 WLEDs With One LCD Backlight

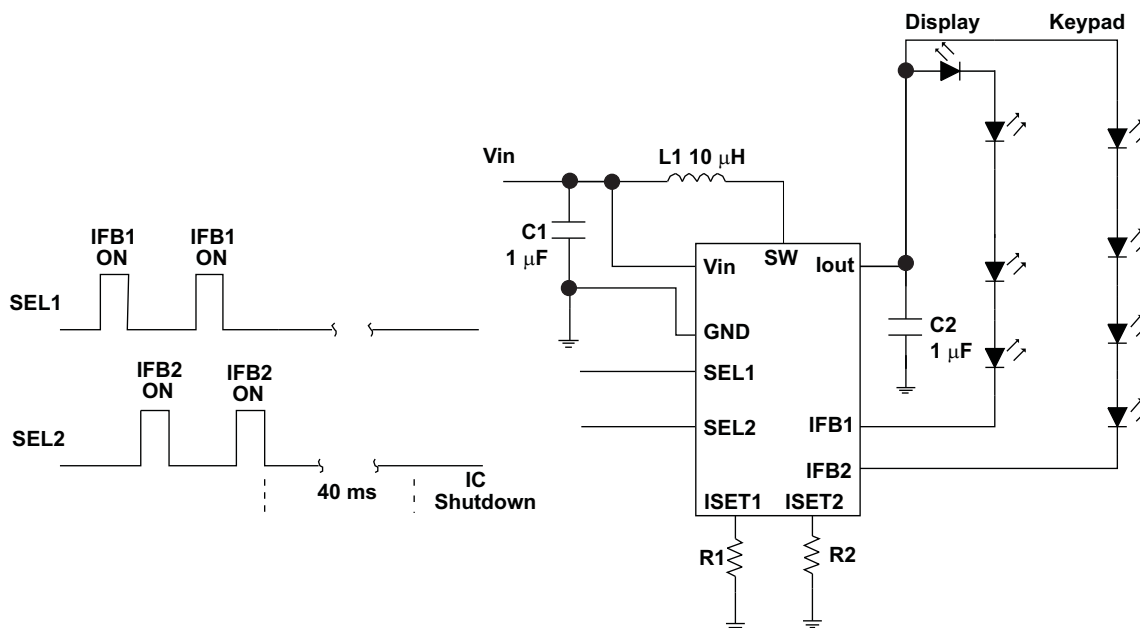


Figure 16. Driving a Keypad and LCD Backlight by applying interleaved PWM signal to the SEL1 and SEL2 pins. The duty cycle of the PWM signal controls brightness dimming

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS61150DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61150DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61150DRCRT	PREVIEW	SON	DRC	10		TBD	Call TI	Call TI
TPS61150DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61150DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61151DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61151DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61151DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61151DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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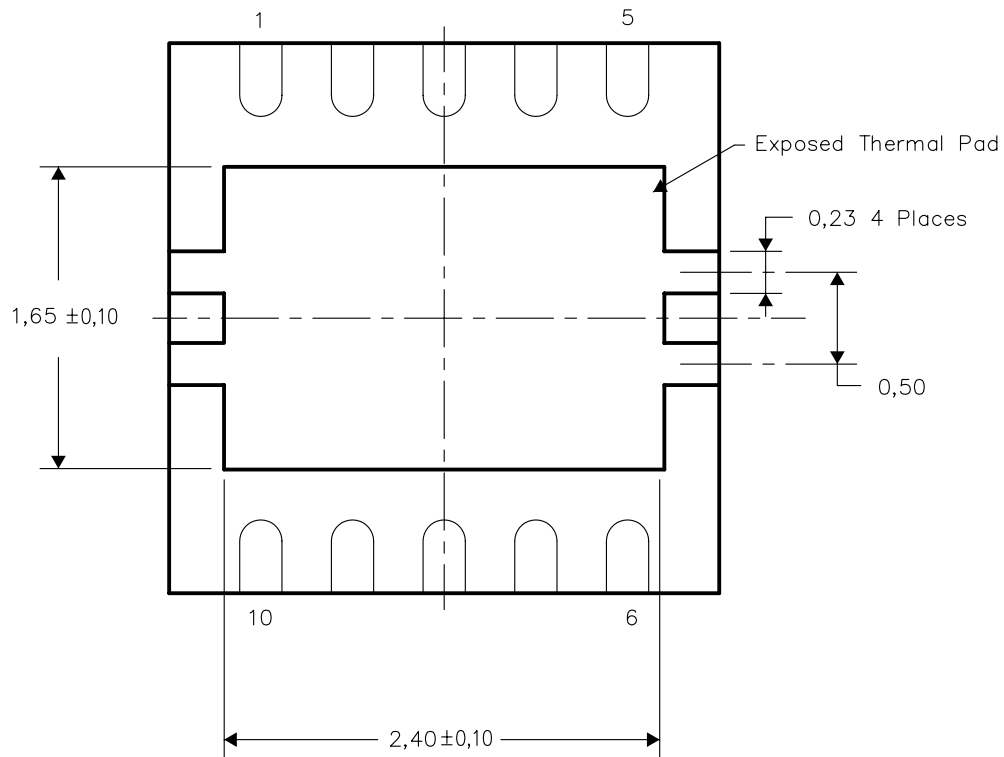
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THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

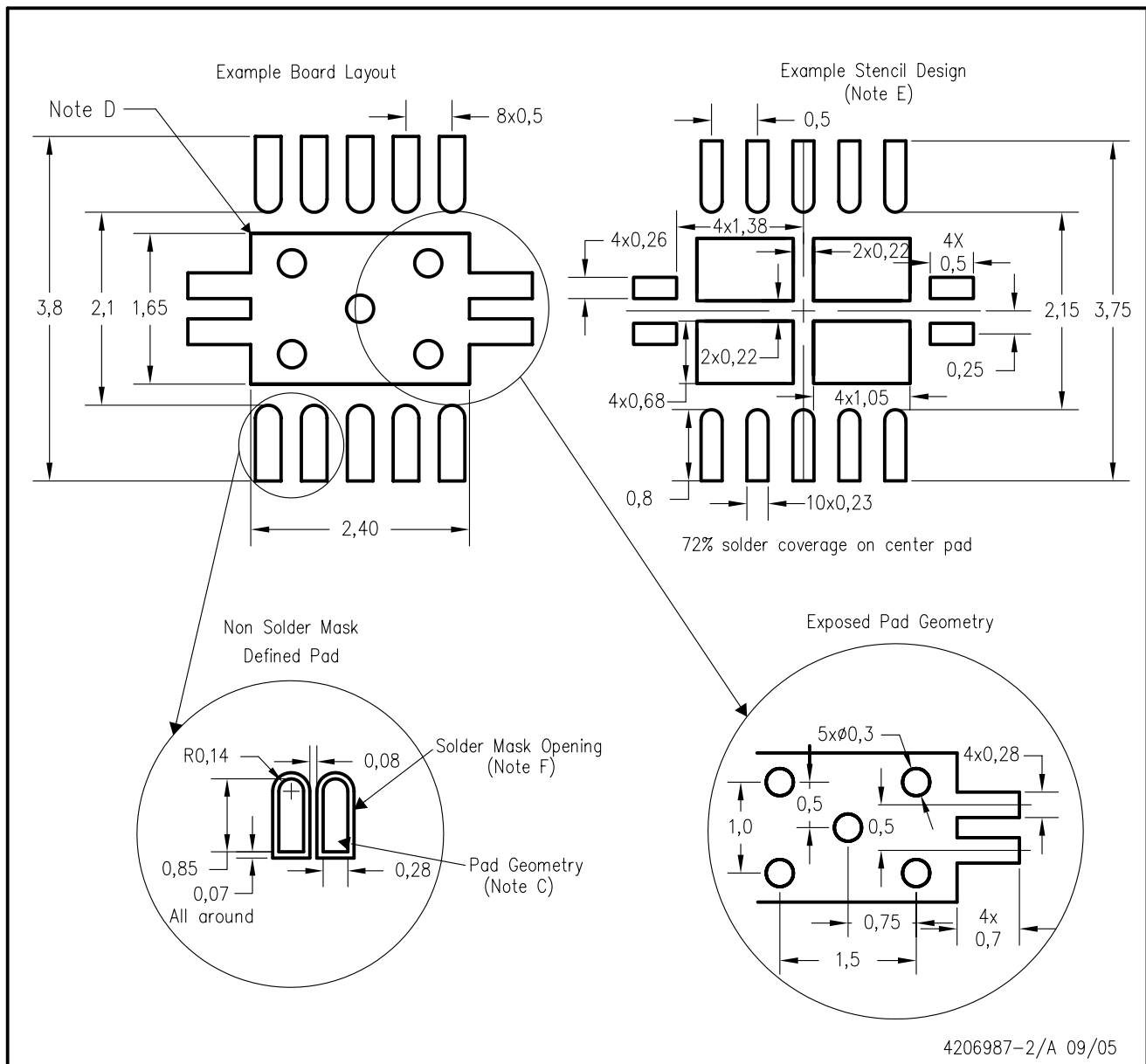


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRC (S-PDSO-N10)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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